TRANSISTOR INCLUDING A DEPOSITED CHANNEL REGION HAVING A DOPED PORTION

CROSS-REFERENCE TO RELATED APPLICATION

This application claims priority from copending application serial number 60/490,239 filed on July 25, 2003, which is hereby incorporated by reference herein.

BACKGROUND

Thin-film transistors and other three-port semiconductor devices typically include gate, source and drain electrodes. A semiconductive thin-film channel is disposed between the source electrode and drain electrode. The transistor also includes a dielectric insulator physically separating the gate electrode from the channel, and from the source electrode and the drain electrode. The semiconductive channel provides an electrical pathway between the source and drain electrodes having controllable conductive properties. In particular, the voltage applied to the gate electrode causes the conductive properties of the channel to vary. Specifically, the applied gate voltage controls the ability of the channel material to permit charge transport through the channel material between the other two electrodes (e.g., a source electrode and drain electrode). The electrical properties of the various materials used in the thin-film transistor determine the threshold voltage required to turn on the transistor and induce a conductive pathway between the source and drain electrodes.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 depicts an embodiment of an exemplary three-port semiconductor device according to the present description, in the form of a thin-film transistor.

Fig. 2 schematically depicts an exemplary embodiment of a thin-film transistor according to the present description in which a portion of the

transistor's channel is doped to vary the threshold gate voltage required to turn on the transistor.

Figs. 3–5 schematically depict further exemplary embodiments of thin-film transistors according to the present description.

Fig. 6 depicts various current-voltage characteristic curves showing variation in threshold voltage that may be achieved by dimensionally varying doped regions within embodiments of the thin-film transistor channels of the present description.

Fig. 7 depicts an embodiment of an exemplary display system in which the thin-film transistor technologies of the present description may be employed.

DETAILED DESCRIPTION

The present description pertains to a system and method involving a multi-port semiconductor device in which a novel configuration is employed in one or more of the charge-carrying portions of the device. The present system and method is applicable to a variety of semiconductor applications, but has proved particularly useful in the context of thin-film transistor (TFT) technologies.

Fig. 1 depicts an exemplary three-port semiconductor device according to the present description, such as thin-film transistor (TFT) 10. As shown, TFT 10 may employ a bottom-gate structure, in which material comprising a gate electrode 12 is disposed adjacent a substrate 14. A dielectric 16 is disposed atop gate 12. A channel layer 18 is interposed between dielectric 16 and source electrode 20 and drain electrode 22. As known in the transistor arts, electrical conditions existing at gate electrode 12 (e.g., a gate voltage applied to port 24) determine the ability of the device to transport charge through channel 18 between source 20 and drain 22 (e.g., as current flowing through the channel between ports 26 and 28).

It will be appreciated that a variety of different fabrication techniques and materials may be employed to fabricate a thin-film transistor, such as that shown in the figure. In the depicted example, substrate 14 may be formed from glass and coated with a material such as indium-tin oxide (ITO) to form the gate electrode. Although the gate electrode and dielectric are depicted as blanket-coated, unpatterned layers in Fig. 1, they may in general be patterned as

appropriate. A channel layer is disposed over the dielectric, as will be explained, and indium-tin oxide contacts are disposed for the source and drain electrodes. Regardless of the particular fabrication techniques, the different regions are disposed/configured so that: the source and drain electrodes are physically separate from one another (e.g., separated by the channel material); the three ports (source, drain and gate) are physically separated from each other (e.g., by the dielectric and channel); and the dielectric separates the gate from the channel.

The ITO source/drain contacts may be deposited via RF sputtering, or through other suitable deposition methods. The source and drain contacts may be disposed via patterning with shadow masks or the like, or through other suitable patterning methods.

Figs. 2-5 depict further embodiments of a thin-film transistor according to the present description. The different exemplary embodiments are respectively depicted as 40, 42, 44 and 46.

Typically, as in the depicted examples, the thin-film transistor will be constructed on a substrate 50, such as glass or another suitable material. Various layers of conductive material, insulative/dielectric material and semiconductive material are deposited and/or patterned to provide conductive electrodes and interposed material having desired electrical characteristics.

For many of the particular fabrication methods or sequences used to create the various portions of the device, typical configurations will include: (a) three primary electrodes, referred to as the gate 60, source 62 and drain 64; (b) a dielectric material 70 interposed between gate electrode 60 and each of the source and drain electrodes 62 and 64, such that dielectric material 70 physically separates the gate from the source and drain; (c) a semiconductive material, referred to as the channel 80, disposed so as to provide a controllable electric pathway between the source electrode and the drain electrode. This general configuration is depicted in each of the examples of Figs. 2-5. In such a configuration, as discussed with reference to the examples discussed above, voltage applied at gate electrode 60 varies the ability of channel 80 to permit electrical charge to move between the source and drain electrodes. The

conductive properties of the channel are thus controlled at least in part through application of a voltage at the gate electrode.

The source, drain and gate electrodes may be fabricated from gold, aluminum or another suitable conductive metal or other material. In many cases, it will be desirable to deposit excess conductive material (e.g., as a blanket layer) and then pattern the electrode as desired using masks, etching and the like. Various different materials may be employed as dielectric 70, though silicon dioxide has proved useful in many settings.

The thin-film examples described herein do not include a channel fabricated from the bulk semiconductor material. Instead, channel 80 typically is deposited as a thin layer immediately adjacent dielectric material 70. Indeed, it will be appreciated that the depictions in the figures are exemplary and are intended to be schematic. The relative dimensions of a device constructed according to the present description, or of its constituent parts, may vary considerably from the relative dimensions shown in the present figures.

For many of the sequences in which channel 80 and source/drain electrodes 62 and 64 are deposited and patterned, the resulting configuration typically is as described above, namely that the channel is positioned so as to provide a controllable charge pathway between the source and drain electrodes, and dielectric 70 physically separates the channel and gate electrode 60. Any suitable semiconductor material may be employed for channel 80. For example, zinc oxide, tin oxide or indium oxide may be used in fabricating the channel. As described in detail below, it may in some cases be desirable to dope this underlying channel material so that an impurity is introduced into a portion of channel 80. Typically, this portion will be a boundary region at or near the interface between the channel and dielectric.

As in the depicted examples, a thin-film transistor according to the present description may take a variety of different configurations. Figs. 2 and 3 show exemplary thin-film transistors having bottom gate configuration. A substrate 50 is employed, though configurations omitting a substrate are possible. Gate electrode 60 is then deposited and patterned as appropriate. Dielectric 70 is deposited on top of the gate electrode and is patterned as necessary. The

channel 80 and source and drain electrodes 62 and 64 are then deposited and patterned as appropriate. In the example of Fig. 2, the source and drain electrodes are formed first, and then channel 80 is deposited on top of the source and drain electrodes. In the example of Fig. 3, channel 80 is deposited first, and the source/drain electrodes are subsequently deposited.

A top gate structure may be employed, as in the examples of Figs. 4 and 5. In such a configuration, a substrate 50 may again be employed, but the source 62, drain 64 and channel 80 are formed prior to depositing of the layers comprising dielectric 70 and gate electrode 60. In the example of Fig. 4, channel 80 is deposited first as a thin film, and source 62 and drain 64 are deposited and patterned on top of the deposited channel layer. In the example of Fig. 5, channel 80 is deposited on top of the already-formed source and drain electrodes 62 and 64. In either case, dielectric 70 is deposited next and patterned as necessary, and gate electrode 60 is deposited and patterned on top of dielectric 70.

It will be appreciated that in the examples discussed herein, the conductive properties of channel 80 (Figs. 2-5) will vary depending upon the voltage applied at gate electrode 60. At a certain gate voltage level, referred to as the turn-on or threshold voltage, the ability of the channel to transport charge in response to an applied potential is activated. At gate voltages below the threshold, the source-drain current in response to a give source-drain potential typically does not change as the gate voltage is increased (or at least the drain current does not significantly increase; see the related discussion of Fig. 7 below). Once the threshold voltage is achieved, however, increases in gate voltage produce a steadily increasing source-drain current.

In certain applications, it will be desirable that the transistor threshold voltage by consistently and reproducibly controlled over some desired range of voltage. Furthermore, it will at times be desirable that the transistor be configured with a threshold voltage of zero volts.

Accordingly, the underlying material of channel 80 may be doped with an impurity in a boundary region 82 at or near the interface between channel 80 and dielectric 70. The impurity typically is selected so as to increase or decrease the

fixed charge introduced within the channel in the doped area. This variation in turn provides variation in the turn-on voltage required to induce a conductive pathway between the source and drain electrodes.

As discussed above, typically only a portion of the channel is doped differently to provide the turn-on voltage variation. Usually the doped area is a boundary portion 82 or region at or near the interface between channel 80 and dielectric 70. One way in which this is achieved is by depositing a distinct layer of differently-doped channel material so that the distinct layer is adjacent to and in contact with dielectric 70 as in the depicted examples of Figs. 2-5. The remaining layer or layers of the channel (e.g., portion 84 in Fig. 2) are fabricated with the same underlying material (e.g., zinc oxide) but are not doped with the additional impurity. Additionally or alternatively, a region of differently-doped material may be achieved by varying certain processing parameters during deposition of the channel layers, so as to achieve a localized region of the channel that is doped differently than the rest of the channel.

The impurity introduced into the boundary region may be a donor-type impurity that interacts with the underlying material so as to increase the positive fixed charged density introduced into the doped region. The higher positive charge density thus lowers the gate voltage required to induce a conductive path between source electrode 62 and drain electrode 64. In the case where zinc oxide is employed as the underlying channel material, aluminum is an example of a suitable donor-type impurity that may be introduced in order to increase the fixed positive charge density within the boundary region 82, and thereby lower the turn-on voltage required at gate electrode 60 to induce conduction between source 62 and drain 64. Other donor-type impurities that may be employed for with underlying zinc-oxide channel include boron, gallium, indium, fluorine and chlorine. The impurities may be incorporated into the device via RF sputtering, DC or ion beam sputtering (e.g., from an oxide target or reactively from a metal target), thermal or e-beam evaporation, chemical vapor deposition, pulsed laser deposition, atomic layer deposition, molecular beam epitaxy and/or other suitable methods.

Acceptor-type impurities may also be employed, so as to increase the fixed negative charge density within the differently-doped region and thereby effect an increase in threshold voltage. As with the donor-type impurities, such variation in doping typically will be implemented only within a portion of the channel, with such portion typically being at or near the interface between channel 80 and dielectric 70. Exemplary acceptor-type impurities that may be used with a zinc-oxide channel include nitrogen, phosphorus, arsenic, antimony, lithium, sodium, potassium and copper.

For an underlying indium oxide channel, acceptable donor-type impurities include silicon, germanium, tin, lead, fluorine and chlorine, while acceptable acceptor-type impurities include nitrogen, phosphorous, arsenic and antimony. For an underlying tin oxide channel, acceptable donor-type impurities include arsenic, antimony, bismuth, fluorine and chlorine, while acceptable acceptor-type impurities include boron, aluminum, gallium, indium, nitrogen, phosphorus, arsenic and antimony.

It has been determined that the obtained variation in threshold voltage varies with the dimensions of the differently-doped portion of channel 80. Fig. 6 depicts various I-V characteristics for doped regions within the channel boundary region having varying thicknesses. The depicted data was obtained using thin-film transistors according to the present description having a width-to-length ratio of 6:1 and using a furnace anneal temperature of 400 degrees Celsius. The underlying channel material employed was zinc oxide, and the different transistors were formed to have a differently-doped interfacial layer within the channel. Aluminum was employed as a donor-type dopant impurity to create the boundary layer adjacent the transistor dielectric material.

Threshold voltage was evaluated by setting the drain-to-source voltage at a fixed value (10 V in the present example) and sweeping the gate voltage. The figure shows transfer curves for four different transistors, where boundary region channel thickness (e.g., of the differently-doped boundary region 82) is 0, 5, 10 and 15 Å, respectively, moving from right to left in the figure. The threshold voltage for each transfer characteristic is indicated with a vertical arrow, at the swept voltage where the drain current begins to increase as a function of

increasing gate voltage. As shown in the figure, threshold voltage V_T decreases by roughly 1 V for each 5 Å in thickness of the differently-doped channel region.

It should be appreciated that the thin-film transistor technologies of the present disclosure may be employed in a variety of different applications. One application includes deployment of a channel with the described selective doping in an active matrix display using thin-film transistors, such as display 100 in Fig. 7. In display applications and other applications, it will often be desirable to fabricate the channel and other device layers to be at least partially transparent.

Referring still to Fig. 7, Exemplary display 100 includes a plurality of display elements, such as pixels 102, which collectively operate to display image data. Each pixel may include one or more thin-film transistors, such as that described above, in order to selectively control activation of the pixels. For example, each pixel may include three thin-film transistors, one for each of a red, blue and green sub-pixel. In such a display, the transistor examples described herein may be employed as a switch to selectively control activation of the sub-pixel.

While the present embodiments and method implementations have been particularly shown and described, those skilled in the art will understand that many variations may be made therein without departing from the spirit and scope defined in the following claims. The description should be understood to include all novel and non-obvious combinations of elements described herein, and claims may be presented in this or a later application to any novel and non-obvious combination of these elements. Where the claims recite "a" or "a first" element or the equivalent thereof, such claims should be understood to include incorporation of one or more such elements, neither requiring nor excluding two or more such elements.